SPECIFICATION

Electronic Version 1.2.8

Stylesheet Version 1.0

METHOD OF CONNECTING CORE I/O PINS TO BACKSIDE CHIP I/O PADS

Background of the Invention

[0001] FIELD OF THE INVENTION The present invention relates to the field of application specific integrated circuits (ASICs); specifically, it relates to a method for connecting core I/O pins to chip I/O pads and more specifically to backside chip I/O pads.

[0002] BACKGROUND OF THE INVENTION With the advance of semiconductor technology, the need for integration to system-on-a-chip (SOC) levels within the ASIC field has increased. While reductions in feature sizes and power supply voltage levels have allowed significant integration improvements, these same integration improvements have made inclusion of complex cores (including analog, mixed signal, memory, and specialty cores) more difficult. For example, certain cores require power supply voltages and/or power consumption levels, which are not compatible with the non-core devices and circuits. Further, while the physical number of interconnection (wiring) levels has increased, the number of physical chip I/Os has become a limiting factor as chip sizes have decreased. Moving from peripheral I/O layout to array I/O layout has also raised new problems. Array I/O allow cores to be positioned anywhere within a chip and designers are placing cores closer to the circuit modules the core supports, raising chip I/O routing and competition issues, power distribution and signal noise issues and modeling and testing issues. These issues impact cost, reliability, design time and overall time to market in a field (ASIC) where cost and time to market are critical concerns.

[0003] FIGs. 1 and 2 are exemplary of the physical features and topography of an SOC ASIC utilizing array chip I/O's and containing a core.

[0004] FIG. 1 is a partial cross-sectional view of a related art integrated circuit chip. In FIG. 1, integrated circuit chip 100 comprises a silicon substrate 105 on which, a multiplicity of interconnection levels 110 are fabricated. Fabricated between silicon substrate 105 and interconnection levels 110 is a device level 115. Interconnection levels 110 include in order above silicon substrate 115, an M1 level 120, an M2 level 125, an M3 level 130, an M4 level 135, an MT level 140 and a passivation level 145. On top of passivation level 145 are chip I/O pads 150 supporting solder balls 155.

[0005] Substrate 105 generally contains the semiconductor portions of devices such as the source, drain, and channels of metal-oxide-silicon (MOS) transistors and device level 115 generally contains the non-semiconductor portions of devices such as the gates of MOS transistors. Each level of interconnection levels 110 includes an insulator, wires formed in the insulator and conductive vias connecting the wires in one level to wires in another level. Interconnect levels 110 wire up devices formed in silicon substrate 105 and device level 115 into circuits and connect those circuits to chip I/O pads 150.

[0006] Contained within chip 100, is a core 160. Core 160 includes portions of silicon substrate 105, device level 115, M1 level 120, M2 level 125 and M3 level 130 that are reserved for core devices and circuits. Core 160 is divided into a core circuit portion 165 and a redistribution portion 170. There are no devices in the portions of silicon substrate 105 and device level 115 contained in redistribution portion 170. There is no wiring in portions of M1 level 120 and M2 level 125 contained within redistribution portion 170. A plurality of core I/O pins 175 are located in redistribution portion 170 at M3 level 130. Global wiring in M3 level 130, M4 level 135, MT level 140 and passivation level 145 electrically connect core I/O pins 175 to chip I/O pads 150.

[0007] FIG. 2 is a partial plan view of the related art integrated circuit chip of FIG. 1. In FIG. 2, core I/O pins 175 of core 160 are electrically connected to chip I/O pads 150 by global wiring 180. The exact routing of global wiring 180 is determined based upon electrical parameter wiring rules such as line resistance and capacitance, power distribution rules limiting voltage drop and current hot-spots and physical wiring rules such as wire width and length matching. While global wiring may be done by software, designs still need to be simulated (tested) and corrections made multiple

times and often by human intervention.

[0008] The present invention provides a method to address chip I/O availability in SOC ASIC chips having cores to minimize cost, design time and overall time to market.

Brief Summary of the Invention

[0009] A first aspect of the present invention is an integrated circuit, comprising: a predefined block of functional circuitry having a plurality of I/O pins; and a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit.

[0010] A second aspect of the present invention is a method of making electrical connection to an integrated circuit, comprising: providing a predefined block of functional circuitry having a plurality of I/O pins; and connecting a backside I/O pad electrically to each I/O pin through a backside via of the integrated circuit.

[0011] A third aspect of the present invention is an electronic device, comprising: (a) an integrated circuit package; (b) an integrated circuit chip comprising: (i) a predefined block of functional circuitry having a plurality of first I/O pins, each first I/O pin electrically connected to a backside I/O pad of the integrated circuit; and (ii) non-predefined functional circuitry having a plurality of second I/O pins, each second I/O pin electrically connected to a frontside I/O pad of the integrated circuit; (c) first connection means for electrically connecting each backside I/O pad to one pad of a first set of package pads; and (d) second connection means for electrically connecting each frontside I/O pad to one pad of a second set of package pads.

[0012] A fourth aspect of the present invention is an electronic device, comprising:(a) a first integrated circuit chip comprising:(i) a predefined block of functional circuitry having a plurality of first I/O pins, each first I/O pin electrically connected to a backside I/O pad of the integrated circuit; and(ii) non-predefined functional circuitry having a plurality of second I/O pins, each second I/O pin electrically connected to a frontside I/O pad of the integrated circuit;(b) a second integrated circuit chip mounted to a back surface of the first integrated circuit chip, the second integrated circuit chip having a plurality of frontside I/O pads; and(c) connection means for electrically connecting each backside I/O pad of the first integrated circuit chip to one frontside

I/O pad of the second integrated circuit chip.

Brief Description of the Several Views of the Drawings

[0013] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[0014] FIG. 1 is a partial cross-sectional view of a related art integrated circuit chip;

[0015] FIG. 2 is a partial plan view of the related art integrated circuit chip of FIG. 1;

[0016] FIG. 3 is a partial cross-sectional view of an integrated circuit chip according to the present invention;

[0017] FIG. 4 is a partial plan view of the integrated circuit chip illustrated in FIG 3, according to the present invention;

[0018] FIGs. 5A through 5D are partial cross-sectional views illustrating fabrication of a backside chip connection according to the present invention;

[0019] FIG. 6 is a partial cross-sectional view illustrating a thinned bulk silicon chip according to the present invention;

[0020] FIG. 7 is a partial cross-sectional view illustrating a silicon-on-insulator (SOI) chip according to the present invention;

[0021] FIG. 8 is a partial cross-sectional view illustrating a thinned SOI chip according to the present invention;

[0022] FIGs. 9 through 11 are partial cross-sectional views illustrating alternative package/chip combinations according to the present invention; and

[0023] FIGs. 12 and 13 are partial cross-sectional views illustrating methods of mounting two chips together according to the present invention.

Detailed Description of the Invention

[0024] In describing the present invention, an exemplary integrated circuit chip utilizing

six interconnection levels and one core will be used. The invention is equally applicable to integrated circuit chips having more or less than six interconnection levels and more than one core. A core includes, in the substrate and interconnect levels, all devices and structures in a specified portion of a chip necessary to perform the function of the core and non-core devices and wiring are excluded from the core. A core is a pre-defined block of functional circuitry contained in a design library and is placed into a chip design that may contain non-predefined circuitry, that is, circuitry designed from non-functional units such as gates. Cores may be as simple as just a driver circuit or as complex as a multi-channel analog to digital converter circuit or a full function embedded content addressable memory (CAM) circuit. Core I/O pins include signal I/O pins, power I/O pins, ground I/O pins and test I/O pins.

[0025] FIG. 3 is a partial cross-sectional view of an integrated circuit chip according to the present invention. In FIG. 3, integrated circuit chip 200 comprises a substrate 205 on which, a multiplicity of interconnection levels 210 are fabricated. Substrate 205 may be a bulk silicon substrate or an SOI substrate. Fabricated between silicon substrate 205 and interconnection levels 210 is a device level 215. Interconnection levels 210 include in order above silicon substrate 215, an M1 level 220, an M2 level 225, an M3 level 230, an M4 level 235, an MT level 240 and a passivation level 245. M1 level 220 is the lowest interconnect level in integrated circuit chip 200. On top of passivation level 245 are frontside chip I/O pads 250 supporting solder balls 255. Solder balls 255 are also called C4 connections, C4 standing for controlled collapse chip connection.

[0026] While five interconnection levels (M1, M2, M3, M4 and MT) are illustrated in integrated circuit chip 200 in FIG. 3, one of ordinary skill in the art would known that more or less interconnection levels may be employed.

[0027]

Substrate 205 contains the semiconductor portions of devices such as the source, drain, and channels of metal-oxide-silicon (MOS) transistors and device level 215 contains the non-semiconductor portions of devices such as the gates of MOS transistors. Each level of interconnection levels 210 includes an insulator, wires formed in the insulator and conductive vias connecting the wires in one level to wires in another level. Interconnect levels 210 wire up devices formed in substrate 205 and

device level 215 into circuits and connect those circuits to chip I/O pads 250.

[0028] Contained within integrated circuit chip 200, is a core 260. Core 260 includes portions of substrate 205, device level 215, M1 level 220, M2 level 225 and M3 level 230 that are reserved for core devices and circuits. Excluded from core 260 are all non-core devices and other structures. Core 260 is divided into a core circuit portion 265 and a redistribution portion 270. Circuit portion 265 includes portions of substrate 205, device level 215, M1 level 220, M2 level 225 and M3 level 230. Circuit portion 265 includes all functional circuitry of core 260. Redistribution portion 270 includes only portions of substrate 205, device level 215 and M1 level 220. There are no devices in the portions of substrate 205 and device level 215 contained in redistribution portion 270. Portions of M2 level 225 and M3 level 230 immediately above redistribution portion 270 are available for wiring to non-core circuits and devices. A plurality of core I/O pins 275 are located in redistribution portion 270 at M1 level 220.

[0029] While three interconnection levels (M1, M2 and M3) are illustrated in core 260 in FIG. 3, one of ordinary skill in the art would known that more or less interconnection levels may be employed.

[0030] Core I/O pins 275 are electrically connected to backside chip I/O pads 280 by conductive backside vias 285 formed in substrate 205, device level 215 and M1 level 220. Each conductive backside via 285 includes an insulating liner 290, a conductive liner 295 and a bulk conductor 300. Insulating liner 290 insulates conductive backside via 285 from substrate 205. Backside chip I/O pads 280 and conductive backside vias 285 are included in the design of core 260 and form part the core.

[0031] FIG. 4 is partial plan view of the integrated circuit chip illustrated in FIG 3, according to the present invention. In FIG. 2, core I/O pins 275 of core 260 are electrically connected to backside chip I/O pads 280 by conductive backside vias 285. Frontside chip I/O pads 250 are free for use by non-core circuits. An optional connection between a core I/O pin 275A to a frontside chip I/O pad 250A by global wiring 305 is also illustrated in FIG. 4 for those cases in which it is desirable to utilize both types of I/O routing for core 260. Core 260 may be placed anywhere within chip 200 irrespective of frontside chip I/O pads 250 availability or demands on the

frontside chip I/O pads by non-core circuits, thus reducing cost, design time and overall time to market.

[0032] FIGs. 5A through 5D are partial cross-sectional views illustrating fabrication of a backside chip connection according to the present invention. In FIG. 5A, substrate 205, device level 215, M1 level 220 and M2 level of integrated circuit chip 200 are illustrated. Within M1 level 220 is a core I/O pin 275. A thick oxide layer 310 is formed on a backside 315 of substrate 205. In one example, thick oxide layer 310 is high-pressure deposition (HDP) oxide or tetraethoxysilane (TEOS) oxide. A via opening 320 is etched (using thick oxide layer 310 as a hard mask) through thick oxide layer 310, substrate 205, device level 215 and partially into the insulating portion of M1 level 220. If substrate 205 is a bulk silicon substrate the substrate may be etched using any one of well-known silicon etch processes such as wet-etch processes utilizing a strong base or a silicon reactive ion etch processes (RIE). If substrate 205 is an SOI substrate, any one of well-known HF containing wet-etch processes or a silicon oxide RIE processes is also used to etch through the insulator portion of the substrate. An SOI substrate is illustrated in FIGs. 7 and 8 and described below.

[0033] In FIG. 5B, insulating liner 290 is formed on sidewalls 325 of via opening 320. Insulating liner 290 extends over thick oxide layer 310. In a first example, insulating liner 290 may be formed from silicon oxide by deposition or oxidation. In a second example, insulating liner 290 may be formed from silicon nitride by deposition.

[0034] In FIG. 5C, portions of insulating liner 290 and M1 level 220 insulator under core I/O pin 275 are removed by any one of well-known RIE processes. A conductive liner 295 is formed over insulating liner 290. In one example, conductive liner 295 is formed from tantalum or titanium by deposition.

[0035] In FIG. 5D, conductive core 300 is formed to complete conductive backside via 285. In a first example, conductive core 300 is copper formed by electroplating followed by a chemical-mechanical-polish (CMP) down to thick oxide layer 310. In a second example, conductive core 300 is tungsten formed by deposition and followed by a CMP down to thick oxide layer 310. Thick oxide layer 310 (see FIG. 5C) is thinned to form thin oxide layer 310A by the CMP process. Backside chip I/O pad 280 is

formed over conductive backside via 285. In one example, backside chip I/O pad 280 is aluminum formed by any one of well-known subtractive etch processes.

[0036] FIG. 6 is a partial cross-sectional view illustrating a thinned bulk silicon chip according to the present invention. In FIG. 6, substrate 205 (see FIG. 5A) is thinned to form thinned substrate 205A before any of the operations illustrated in FIGs. 5A through 5D and described above are performed. Thinning substrate 205 (see FIG. 5A) facilitates formation of via opening 320 (see FIG. 5A). Thinning of substrate 205 (see FIG. 5A) may be accomplished by any one of well-known methods of wet etching in strong basic solutions or by any one of well-known grinding/polishing processes.

[0037] FIG. 7 is a partial cross-sectional view illustrating a SOI chip according to the present invention. In FIG. 7, SOI substrate 205B includes a lower silicon layer 330, a middle buried oxide layer (BOX) 335 and an upper silicon layer 340 in which devices are fabricated. Conductive backside via 285 is formed through BOX layer 335.

[0038] FIG. 8 is a partial cross-sectional view illustrating a thinned SOI chip according to the present invention. . In FIG. 8, substrate 205 (see FIG. 5A) is thinned to form thinned SOI substrate 205C before any of the operations illustrated in FIGs. 5A through 5B and described above are performed. Thinning substrate 205 (see FIG. 5A) facilitates formation of via opening 320 (see FIG. 5A). Thinning of substrate 205 (see FIG. 5A) may be accomplished by any one of the well-known methods of wet etching in strong basic solutions or grinding/polishing processes. Only lower silicon layer 330 (see FIG. 7) is thinned to produce thinned lower silicon layer 330A.

[0039] FIGs. 9 through 11 are partial cross-sectional views illustrating alternative package/chip combinations according to the present invention. FIG. 9 illustrates direct coupling of cores to the package. In FIG. 9, a package 350A has C4 pads 355 for electrical connection of solder balls 255 of integrated circuit chip 200 to solder balls 360 by conductive interconnect structures 365. Package 350A also has wirebond pads 355A electrically connected to solder balls 360A by conductive interconnect structures 365A. Backside chip I/O pads 280 from cores 260 in integrated circuit chip 200 are electrically connected to wirebond pads 355A by wirebond wires 370A. In one example, package 350A is a multilevel ceramic (MLC) package and conductive interconnect structures 365 and 365A include conductive lands and vias. While

package 350A is a ball grid array (BGA) package, other package types such as pin grid arrays (PGA) and solder column arrays (SCA) may be used.

[0040] FIG. 10 illustrates indirect coupling of cores to the package. In FIG. 10, a package 350B has C4 pads 355 for electrical connection solder balls 255 of integrated circuit chip 200 to solder balls 360 by conductive interconnect structures 365. Package 350B also has additional C4 pads 355B electrically connected to solder balls 360B by conductive interconnect structures 365B. A second chip 375 having backside wirebond pads 380 is electrically connected by solder balls 385 to C4 pads 355B. Backside chip I/O pads 280 from cores 260 in chip 200 are connected to backside wirebond pads 380 of second chip 375 by wirebond wires 370B. In one example, package 350B is a multilevel ceramic (MLC) package and conductive interconnect structures 365 and 365B include conductive lands and vias. While package 350B is a ball grid array (BGA) package, other package types such as pin grid arrays (PGA) and solder column arrays (SCA) may be used. Also second chip 375 is defined to include chips having active and/or inactive devices, chips having only conductive interconnect structures and interposers. Interposers may be formed from silicon, quartz, ceramic or other materials known in the art.

[0041] In FIG. 11, both types of connections, direct connection of cores to the package as illustrated in FIG. 9 and described above and indirect connection of cores to the package as illustrated in FIG. 10 and described above are combined in a single package.

[0042] In FIG. 11, a package 350C has C4 pads 355 for electrical connection of solder balls 255 of integrated circuit chip 200 to solder balls 360 by conductive interconnect structures 365. Package 350C also has wirebond pads 355A electrically connected to solder balls 360A by conductive interconnect structures 365A. Backside chip I/O pads 280A from core 260A in integrated circuit chip 200 are electrically connected to wirebond pads 355A by wirebond wires 370A.

[0043] Also in FIG. 11, package 350C has C4 pads 355B electrically connected to solder balls 360B by conductive interconnect structures 365B to solder balls 360B. A second chip 375 having backside wirebond pads 380 electrically connected to solder balls 385 is electrically connected to C4 pads 355B by the solder balls. Backside chip I/O

pads 280B from cores 260B in integrated circuit chip 200 are connected to backside wirebond pads 380 of second chip 375 by wirebond wires 370B.

[0044] FIGs. 12 and 13 are partial cross-sectional views illustrating methods of mounting two chips together according to the present invention. In FIG. 12, integrated circuit chip 200 includes core 260 having backside chip I/O pads 280. A second chip 390 having frontside I/O pads 395 is electrically connected to backside chip I/O pads 280 by C4 balls 400. In FIG. 13, integrated circuit chip 200 includes core 260 having backside chip I/O pads 280. A second chip 405 having frontside I/O pads 410 is electrically connected to backside chip I/O pads 280 by wirebond wires 415.

[0045] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.